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MSLIN-98-002CCCIP_CIPB

February 1, 2006

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, NY 12603

Subject: Serial No. 10/783,195 02/20/04

Mou-Shiung Lin, et al.

TOP LAYERS OF METAL FOR HIGH PERFORMANCE IC'S

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February 6, 2006.

Stephen B. Ackerman, Reg. # 37761

Signature/Date 2/6/06

U.S. Patent 6,229,221 to Kloen et al., "Integrated Circuit Device," discloses an integrated circuit device.

U.S. Patent 5,719,448 to Ichikawa, "Bonding Pad Structures for Semiconductor Integrated Circuits," discloses a bonding pad structure for a semiconductor integrated circuit which permits miniaturization of the bonding pad size by utilizing an opening in an overlying insulating layer to an exposed surface of an underlying multi-layer, interconnecting wiring of the integrated circuit, constituting a bonding pad for exposure to wire bonding.

U.S. Patent 6,710,460 to Morozumi, "Semiconductor Devices and Methods for Manufacturing the Same," discloses a method for manufacturing a semiconductor device in which wiring layers are formed by a damascene method.

U.S. Patent 5,384,488 to Golshan et al., "Configuration and Method for Positioning Semiconductor Device Bond Pads Using Additional Process Layers," discloses a semiconductor chip which includes a plurality of bond pads.

U.S. Patent 6,800,555 to Test et al., "Wire Bonding Process for Copper-Metallized Integrated Circuits," discloses a robust, reliable and low-cost metal structure and process enabling electrical wire/ribbon connections to the interconnecting copper metallization of integrated circuits.

U.S. Patent Application Publication US 2002/0158334 A1 to Vu et al., "Microelectronic Device Having Signal Distribution Functionality of an Interfacial Layer Thereof," discloses a microelectronic device which includes a microelectronic die having an interfacial metal layer deposited over an active surface thereof to perform a signal distribution function within the device.

U.S. Patent 6,459,135 to Basteres et al., "Monolithic Integrated Circuit Incorporating an Inductive Component and Process for Fabricating Such an Integrated Circuit," discloses a monolithic integrated circuit incorporating an inductive component.

U.S. Patent 6,544,880 to Akram, "Method of Improving Copper Interconnects of Semiconductor Devices for Bonding," discloses an improved wire bond with the bond pads of semiconductor device and the lead fingers of lead frames or an improved conductor lead of a TAB tape bond with the bond pad of a semiconductor device.

U.S. Patent 5,789,303 to Leung et al., "Method of Adding On Chip Capacitors to an Integrated Circuit," discloses a capacitor structure and method of forming a capacitor structure for an integrated circuit.

U.S. Patent 6,184,143 to Ohashi et al., "Semiconductor Integrated Circuit Device and Fabrication Process Thereof," discloses a semiconductor integrated circuit wherein an interlayer insulating film is formed over a semiconductor substrate having a semiconductor device formed thereover.

U.S. Patent 5,659,201 to Wollesen, "High Conductivity Interconnection Line," discloses high conductivity interconnection lines formed of high conductivity material, such as copper, employing barrier layers impervious to the diffusion of copper atoms.

U.S. Patent 6,187,680 to Costrini et al., "Method/Structure for Creating Aluminum Wirebound Pad on Copper BEOL," discloses a method for fabricating an integrated circuit (IC) structure having an Al contact in electrical communication with Cu wiring embedded in the initial semiconductor wafer.

U.S. Patent 5,969,424 to Matsuki et al., "Semiconductor Device with Pad Structure," discloses a semiconductor device equipped with secondary pads having adequate arrangement for an arbitrary packaging process.

U.S. Patent 6,272,736 to Lee, "Method for Forming a Thin-Film Resistor," discloses a method for forming a thin-film resistor.

U.S. Patent 6,383,916 to Lin, "Top Layers of Metal for High Performance IC's," discloses a method of closely interconnecting integrated circuits contained within a semiconductor wafer to electrical circuits surrounding the semiconductor wafer.

U.S. Patent 6,649,509 to Lin et al., "Post Passivation Metal Scheme for High-Performance Integrated Circuit Devices," discloses a new post-passivation metal interconnect scheme provided over the surface of a IC device that has been covered with a conventional layer of passivation.

U.S. Patent 6,756,295 to Lin et al., "Chip Structure and Process for Forming the Same," discloses a chip structure which comprises a substrate, a first built-up layer, a passivation layer and a second built-up layer.

U.S. Patent 6,593,649 to Lin et al., "Methods of IC Rerouting Option for Multiple Package System Applications," discloses a new method for the creation of Input/Output connection points to a semiconductor device package.

U.S. Patent 6,495,442 to Lin et al., "Post Passivation Interconnection Schemes on Top of the IC Chips," discloses a new method for the creation of interconnect lines.

U.S. Patent 6,455,885 to Lin, "Inductor Structure for High Performance System-On-Chip Using Post Passivation Process," discloses methods of creating high performance electrical components (such as inductor) on the surface of a semiconductor substrate by reducing the electromagnetic losses that are typically incurred in the surface of the substrate.

U.S. Patent 6,103,552 to Lin, "Wafer Scale Packaging Scheme," discloses a process and a package for achieving wafer scale packaging.

U.S. Patent 6,350,705 to Lin, "Wafer Scale Packaging Scheme," discloses a process and a package for achieving wafer scale packaging.

U.S. Patent 5,468,984 to Efland et al., "ESD Protection Structure Using LDMOS Diodes with Thick Copper Interconnect," discloses an interconnection structure and method for a multiple zener diode ESD protection circuit for power semiconductor devices.

U.S. Patent 6,020,640 to Efland et al., "Thick Plated Interconnect and Associated Auxillary Interconnect," discloses a thick plated interconnect comprising a copper lead and a bonding cap coupled to the copper lead.

U.S. Patent Application Publication US 2001/0035452 A1 to Test et al., "Wire Bonding Process for Copper-Metallized Integrated Circuits," discloses a robust, reliable and low-cost metal structure and process enabling electrical wire/ribbon connections to the interconnecting copper metallization of integrated circuits.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
MSLIN98-002CCCIP-CIPB	10/783,195
Applicant: M.S. Lin et al.	
Filing Date: 02/20/04	Group Art Unit:

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6229221	5/8/01	Kloen et al.	257	784	12/6/99
	5719448	2/17/98	Ichikawa	257	781	10/26/93
	6710460	3/23/04	Morozumi	257	779	6/3/02
	5384488	1/24/95	Golshan et al.	257	786	10/3/93
	6800555	10/5/04	Test et al.	438	687	3/23/01
	6459135	10/1/02	Basteres et al.	257	528	3/15/00
	6544880	4/8/03	Akram	438	617	6/14/99
	5789303	8/4/98	Leung et al.	438	381	7/11/96
	6184143	2/6/01	Ohashi et al.	438	697	7/28/98
	5659201	8/19/97	Wollesen	257	758	6/5/95
	6187680	2/13/01	Costrini et al.	438	688	10/7/98

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

–	U.S. Patent App. Pub. US 2002/0158334 A1 to Vu et al, U.S. Cl. 257/723, Pub. Date 10/31/02, Filed 4/30/01.
–	U.S. Patent App. Pub. US 2001/0035452 A1 to Test et al., U.S. Cl. 228/180.5, Pub. Date 11/1/01, Filed 3/23/01

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

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	5969424	10/19/99	Matsuki et al.	257	768	12/29/97
	6272736	8/14/01	Lee	29	620	11/13/98
	6383916	5/7/02	Lin	438	637	2/17/99
	6649509	11/18/03	Lin et al.	438	618	10/24/01
	6756295	6/29/04	Lin et al.	438	612	4/15/02
	6593649	7/15/03	Lin et al.	257	697	5/17/01
	6495442	12/17/02	Lin et al.	438	618	10/18/00
	6455885	9/24/02	Lin	257	300	10/3/01
	6103552	8/15/00	Lin	438	113	8/10/98
	6350705	2/26/02	Lin	438	779	7/14/00
	5468984	11/21/95	Efland et al.	257	356	11/2/94

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6020640	2/1/00	Efland et al.	257	751	12/17/97

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